REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow. At the time of the outstanding Office Action, claims 1-16 were pending. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

Prior Art Rejections:

Claims 1-3, 7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,630,056 to Horvath et al. (hereinafter "Horvath"). Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath in view of U.S. Patent 6,496,940 to Horst et al. (hereinafter "Horst"). Claims 5, 6, 8-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath in view of U.S. Patent 4,860,119 to Maniwa et al. (hereinafter "Maniwa"). These rejections are traversed for at least the following reasons. Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The invention as claimed teaches an apparatus that has a plurality of reception interface sections "which receive **same data from a same data sender**" in parallel, wherein, "upon occurrence of an error in said received data, stops receiving said data, **sends a communication error signal to other reception interface sections to stop data reception from said data sender**, and requests said data sender to resend data." (Independent claim 1, emphasis added; similar language appears in independent claims 7 and 12)

Claims 1-3, 7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Horvath. Horvath fails to teach an apparatus with reception interface sections that receive the same data from a same data sender in parallel. The Examiner points to the following section of Horvath to teach this feature:

> "The invention provides, in one aspect, a digital data processing device that includes a bus for **transmitting signals** (e.g., data and/or address information) **between plural functional units** (e.g., a central processing unit and a peripheral controller). A first such unit includes first and second

> processing sections that **concurrently apply to the bus complementary portions of like information signals** (e.g., longwords containing data)." (column 2, lines 25-32, emphasis added)

Further, the Examiner, in the Response to Arguments, specifically points to the following section of Horvath to teach that the same data is received in parallel at a plurality of different reception interface sections:

> "The functional units can operated in duplex for lock-step redundant processing. Thus, **illustrated processor/memory elements 10, 12 are partnered with one another to respond concurrently and identically to information input from bus 20** to generate further information for output to bus 20. Likewise, illustrated peripheral device controllers 14, 16 are partnered with one another to process and communicate like information between the functional units and peripheral devices (not shown)." (column 3, line 60 to column 4, line 2, emphasis added)

Applicants respectfully submit that Horvath teaches parallel processing, which enables concurrently processing information received from a data source (in this case a bus). The parallel processing can provide identical processing of data. However, there is no indication or teaching in Horvath that the data input from the bus and received at the processor/memory elements is the same data. Processing data concurrently and identically is in no way equivalent to receiving the same data from the same data sender. Thus, Applicants respectfully submit that Horvath fails to teach or disclose an apparatus that has a plurality of reception interface sections" which receive **same data from a same data sender**" in parallel.

Further, the Examiner cites Horvath to teach the feature of sending a signal to stop data reception from the offending data sender to other reception interface sections:

> "A fault detection element reads the resultant signal from the bus and compares it with at least portions of the corresponding signals originally generated by the processing sections themselves. If there is discrepancy, the fault-detector signals a fault." (column 2, lines 32-36)

> "According to a related aspect of the invention, the first functional unit can respond to a processing error by disabling the first and second processing sections from applying further signals to the bus. The processing sections, moreover, can respond to a transmission error by reapplying respective portions of certain prior information signals to the bus. " (column 2, lines 47-53)

The Examiner asserts that these passages teach that "upon detection of error, functional unit disabling the processing section further from applying signals and responding to the error by reapplying the data." (Office Action, page 16, lines 6-8). However, the invention as claimed requires that, "upon occurrence of an error in said received data, stops receiving said data, **sends a communication error signal to other reception interface sections to stop data reception from said data sender**, and requests said data sender to resend data." In the cited sections, Horvath teaches disabling the processing sections of a single apparatus that detected the error, and sending a transmission error to the bus. There is no teaching or suggestion in this cited section, or anywhere in Horvath, that a signal is sent to other reception interface sections to stop data reception from the data sender. Disabling processing sections from applying further signals to the bus is not equivalent to sending a signal to another interface section to tell them of a communication error.

Thus, Horvath fails to teach all of the features of the invention as claimed in independent claims 1, 7 and 12, specifically failing to teach an apparatus that, "upon occurrence of an error in said received data, stops receiving said data, **sends a communication error signal to other reception interface sections to stop data reception from said data sender**, and requests said data sender to resend data." (emphasis added). If this rejection is maintained, the Examiner is respectfully requested to point out where these features are found in Horvath.

The dependent claims are also patentable for at least the same reasons as the independent claims on which they ultimately depend. In addition, they recite additional patentable features when considered as a whole. As mentioned above, Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath in view of Horst. Horst fails to make up for the deficiencies of Horvath as detailed above. Specifically, Horst teaches:

> "Error-checking of the communication flow between the components of the processing system is achieved by adding a cyclic-redundancy-check (CRC) to the message packets, that are sent between the elements of the system. The CRC of each message packet is checked not only at the destination of the message, but also while en route to the destination by each router element used to route the message packet from its source to the destination. **If a message packet is found by a router element to have an incorrect CRC, the message packet is tagged as such, and reported to a maintenance diagnostic system**. This feature provides a useful tool for fault isolation. **Use of CRC in this manner operates to protect message packets from end to end because the router elements do not modify or regenerate the CRC as the message packet passes through**. The CRC of each message packet is checked at each router crossing. A command symbol—"This packet Good" (TPG) or "This Packet Bad" (TPB)—is appended to every packet. **A maintenance diagnostic processor can use this information to isolate a link or router element that introduces an error, even if the error was transient**." (column 5, lines 34-54; emphasis added)

There is no teaching or suggestion in this passage, or anywhere else in the disclosure of Horst, that an apparatus, "upon occurrence of an error in said received data, stops receiving said data, **sends a communication error signal to other reception interface sections to stop data reception from said data sender**, and requests said data sender to resend data." (emphasis added). If this rejection is maintained, the Examiner is respectfully requested to point out where these features are found in either Horvath, Horst, or any combination thereof.

Claims 5, 6, 8-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horvath in view of Maniwa. Maniwa fails to make up for the deficiencies of Horvath as detailed above.

First, Applicants submit that Maniwa and Horvath are not analogous art. Horvath is directed towards a digital data processing device and fault detection and fault tolerance methods. Maniwa is directed towards an image forming system with memory duplex printing that is capable of printing on both sides of a sheet at increased speed. Applicants submit that one of ordinarily skill in the art of parallel data processing, the field of the invention, would not think it obvious to look to the field of image formation and printing to combine teachings to augment those teachings found in field of parallel data processing. Thus, the rejection under 103(a) of claims 5, 6, 8-11 and 13-16 over Horvath in view of Maniwa is not valid.

Further, even if Maniwa were to be incorrectly combined with Horvath, Maniwa fails to make up for the deficiencies of Horvath as detailed above. There is no teaching or suggestion in Maniwa of an apparatus that has a plurality of reception interface sections "which receive **same data from a same data sender**" in parallel, wherein, "upon occurrence of an error in said received data, stops receiving said data, **sends a communication error signal to other reception interface sections to stop data reception from said data sender**, and requests said data sender to resend data." (Independent claim 1, emphasis added; similar language appears in independent claims 7 and 12)

Maniwa fails to mention sections that receive same data from a same data sender. Further, although Maniwa teaches error correction, there is no teaching or suggestion that upon receiving an error in **received data**, a communication signal is sent to other reception interface sections to stop data reception. Rather Maniwa teaches:

> "When an error regarding the printer engine occurs, the printer ceases all the functions thereof. When an error regarding the printer controller occurs, **information on the raised error except for a fatal error is stacked in an error history memory until the error is reset.**" (column 10, lines 49-54 ; emphasis added)
>
> "When the printer controller 130 receives the response from the printer engine unit 90, if a communication error occurs or a response having an unclear meaning is received, **the printer controller 130 sends the identical command to the printer engine unit 90 again**. However, if a

> communication error occurs again or a response having an unclear meaning is received again, **the printer controller 130 stops the communication or sends an initialization command to the printer engine unit 90.**" (column 39, lines 12-20; emphasis added)

Thus, there is no teaching or suggestion in these passages, or anywhere else in the disclosure of Maniwa, of an apparatus that, upon receiving an error is received data, a communication signal is sent to other reception interface sections to stop data reception.

Further, Maniwa teaches diagnosis and service functions, which include error checking at startup of the printer. (column 42, line 1 to column 44, line 37) There is no teaching or suggestion in these functions that upon receiving an error in received data, a communication signal is sent to other reception interface sections to stop data reception.

Thus, Maniwa also fails to teach all of the features of independent claims 1, 7 and 12. As mentioned above, Horvath also fails to teach all of the features of independent claims 1, 7 and 12. If this rejection is maintained, the Examiner is requested to point out where these features can be found in Horvath, Maniwa, or any combination thereof.

The Examiner also cites the combination of Horvath with Maniwa to teach the features of independent claim 6. Specifically, the Examiner cites Horvath to teach the feature of "a data processing apparatus that has a transmission interface section which transmits transmission data to a plurality of data receivers at a same timing:"

> "The invention provides, in one aspect, a digital data processing device that includes a bus for transmitting signals (e.g., data and/or address information) between plural functional units (e.g., a central processing unit and a peripheral controller)." (column 2, lines 25-29 of Horvath).

However, there is no teaching or suggestion in this passage that the transmission data is transmitted to the plurality of data receivers at a same timing. Horvath merely teaches a device that includes a bus for transmitting signals between plural functioning units. There is no teaching or suggestion herein, or anywhere in the disclosure of Horvath, that the transmission of data to a plurality of data receivers is done at a same timing, as required by the invention as claimed. Further, the Examiner refers to the teaching of Horvath that the first

and second processing sections route signal to the bus and, conversely, to the fault-detector. (column 2, lines 54-59). Routing signals to a bus and, conversely, to a fault-detector is in no way equivalent to transmitting data to a plurality of receivers at a same timing. There is no teaching or disclosure in Horvath that the signals are routed to both the bus and the fault-detector at the same time. Thus, Horvath fails to teach all of the features of the invention as claimed.

Maniwa fails to make up for these deficiencies of Horvath. Maniwa fails to teach that data is transmitted to a plurality of data receivers at a same timing. The Examiner cites Maniwa to teach that "a data processing apparatus wherein transmission interface generating packet data by dividing data to data of a data length sendable within one period of a predetermined clock signal and sending that generated data to said plurality of receivers at the same timing in synchronism with said clock signal." (page 9, line 17 to page 10, line 2). Specifically, the Examiner cites the following passage from Maniwa:

> "As shown in FIG. 17, the address controller 141 comprises a direct memory access (DMA) address controller 180, a video address controller 181, a refresh address counter 182 and a selector 183. The DMA address controller 180 controls a DMA address which is used for forming the video data in the video buffer 194 (FIG. 19) provided in the RAM 133 on the basis of the data stored in the page buffer 193 also provided therein. The video address controller 181 is used for **sequentially outputting the video data formed in the video buffer 194 in synchronism with the video clock (WCLK)**. The refresh address counter 182 controls the refreshing operation for the RAM 133. The selector 183 selects one of the output signals from the DMA address controller 180, video address controller 181 and the refresh address counter 182 at a time when the switching is necessary." (column 18, lines 24-63; emphasis added)

Thus, Maniwa teaches sequentially outputting video data in sync with the video clock. However, Maniwa fails to teach a plurality of receivers, or that data is sent to a plurality of receivers in sync with the clock signal, and at a same timing. Rather, Maniwa teaches that one transmission of data is output during one clock cycle. This is in contrast to the invention

as claimed, which requires that transmission data is sent to a plurality of data receivers at a same timing, wherein the packet data is generated by dividing the transmission data to data of a data length sendable within one period of a predetermined clock signal and sends individual pieces of packet data generated to said plurality of data receivers at the same timing in synchronism with said clock signal. There is no teaching or suggestion in Maniwa of such a data transmission.

As shown, Maniwa fails to teach all of the features of independent claim 6. As mentioned above, Horvath also fails to teach all of the features of independent claim 6. If this rejection is maintained, the Examiner is requested to point out where these features can be found in Horvath, Maniwa, or any combination thereof.

Conclusion:

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing or a credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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